16. (Amended) The computer readable medium of claim 13, further comprising the step of performing power analysis prior to the step of performing verification analysis on the derivative circuit design.

17. (Amended) The computer readable medium of claim 13, wherein only a set of new functionality added to the original circuit design and any functionality interfacing with the set of new functionality is tested or verified.

18. (Amended) The computer readable medium of claim 13, wherein step (a) through step (e) are repeated to create a second derivative circuit design, such that the original circuit design comprises a derivative circuit design.

19. (Amended) The computer readable medium of claim 13, wherein the step of planning the chip layout comprises analyzing timing requirements to ensure the derivative circuit design meets all applicable timing requirements.

20. (Amended) The computer readable medium of claim 13, further comprising the step of assembling a chip based on the chip layout prior to the step of performing verification analysis on the derivative circuit design.

22. (Amended) The computer readable medium of claim 21, wherein each of the one or more programmable fabrics has a port access and hierarchical routing.

REMARKS

Claims 2-23 are pending in the subject application. Applicants respectfully request entry of the amendments to the specification, drawings, and claims. The amendments correct typographical and clerical errors, insert information not previously available, and further clarify the invention. Thus, the amendments merely correct informalities and are not intended to limit the scope of the invention or overcome any cited prior art. No new matter has been added.

Information Disclosure Statement

The Office action states:

> Although the information disclosure statement filed 13 April 2001 complies with the provisions of 37 C.F.R. 1.97, 1.98 and MPEP § 609, some of the references are currently not considered because they cannot be found in the parent application. Examiner requested a duplicate of the references . . . .

Enclosed herein is a copy of the initialed Form-1449 from the parent application, Serial No. 09/410,356, showing receipt of those references by the U.S. Patent and Trademark Office. As a courtesy, the references cited in the parent application that cannot be found in the parent file are included with the supplemental information disclosure statement filed herewith.

Objections to Drawings

According to the Office Action, Figure 25 contains a typographical error. A proposed drawing correction is submitted together with this response. Applicants believe that the proposed change to the drawing, if entered, would overcome the above objection.

Objections to Specification

The Office Action objected to the specification on the basis of informalities. Applicants have amended the specification to correct those informalities. Therefore, Applicants respectfully submit that the objections have been traversed.

Objections to Abstract

The abstract was objected to on the grounds that it exceeds 300 words. Applicants respectfully submit that the abstract does not exceed the 150-word limit allowed under 37 C.F.R. § 172(b). Accordingly, Applicants respectfully request withdrawal of the objection.

Objections to Claims

Claims 2, 6-7, 9, 11, 13, 17-18, and 20 have been objected to because of informalities. Applicants believe that the claims as amended would overcome objections. Thus, withdrawal of the objections is respectfully requested.

Claim Rejections under 35 U.S.C. § 112, ¶ 2

Claims 3, 7, 9, 14, 18, and 20 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Applicants believe that the claims as amended traverse the rejection. Hence, Applicants respectfully request withdrawal of the rejection.

Claim Rejections under 35 U.S.C. § 103(a)

Claims 2-23 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Miller et al., U.S. Patent No. 6,175,948 (hereinafter "Miller"), in view of Dawid, Herbert et al., "ADAPCM Codec: From System Level Description to Versatile HDL Model" (hereinafter "Dawid"). Applicants respectfully traverse the rejection.

Miller is directed to "a waveform compiler that provides waveform application development, allows partitioning of that application functionality to a target architecture, and further provides a way of generating and optimizing code and ancillary target software for use in communication systems." (Col. 2, ll. 11-15). The invention in Miller allows for design and coding of a software application that is optimized for the target platform, i.e., the hardware, the application will be executed on. (Col. 4, ll. 44-46).

In contrast, amended claim 2 is directed to "[a] method for creating a derivative circuit design." The passage of Miller cited in the Office Action merely states that the application modules created using the methodology disclosed are designed "with reuse as a key design consideration to provide code generation and synthesize internal structure into optimized target executable code." (Col. 5, ll. 43-45). Thus, Miller does not disclose "[a] method for creating a derivative circuit design" as recited in claim 2.

Miller also fails to disclose or suggest the steps of: "selecting an original circuit design, wherein the original circuit design comprises one or more programmable fabrics"; "performing front-end acceptance testing on the original circuit design"; "planning a chip layout"; "programming at least one of the one or more programmable fabrics to create a derivative circuit design"; and "performing verification analysis on the derivative circuit design" as recited in amended claim 2.

The passages of Miller cited in the Office Action relate to the flow diagram of Fig. 2, which merely describes how a software application for a specific target platform is designed and coded. (Col. 5, l. 46 to col. 6, l. 54; Fig. 2). Therefore, Applicants respectfully submit that Miller does not teach each and every element of claim 2.

The Office Action has not identified any passage of Dawid that cures the deficiencies of Miller. Accordingly, claim 2 is believed to be allowable over the combination of Miller and Dawid. Claims 3-12, which depend from claim 2, should be allowable for at least the same reasons. In addition, claims 13-23, which recite claim elements similar to those in claims 2-12, should likewise be allowable for at least the same reasons. Consequently, Applicants respectfully request withdrawal of the rejection and allowance of claims 2-23.

CONCLUSION

On the basis of the above remarks, reconsideration and allowance of the claims is believed to be warranted and such action is respectfully requested. If the Examiner has any questions or comments, the Examiner is invited to contact the undersigned at the number listed below.

Respectfully submitted,

Bingham McCutchen LLP

Dated: 12-3-02

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Enclosures: Marked up version of replacement paragraphs pursuant to 37 C.F.R. § 121(b)(1)(iii).
Marked up version of amended claims pursuant to 37 C.F.R. § 121(c)(1)(ii).
Substitute sheet for FIG. 25.
Drawing sheet for FIG. 25 showing proposed change.
Initialed Form-1449 from Application Ser. No. 09/410,356.

VERSION WITH MARKINGS TO SHOW CHANGES

In the Specification

Paragraph 1 on page 1 is amended as follows:

This application is a continuation-in-part of co-pending U.S. [Provisional]Patent Application Ser. No. 09/410,356, filed on September 30, 1999, now U.S. Patent No. 6,269,467, and also claims priority to U.S. Provisional Patent Application Ser. No. 60/102,566, filed on September 30, 1998, both of which [applications]are incorporated herein by reference in their entireties.

Paragraph 5 on page 2 is amended as follows:

(2) Chip designs are becoming more application-specific. In the early days of IC design, device manufacturers would typically produce various "off-the-shelf" chips, which end users would design into their electronic products. Currently, electronic product manufacturers often order custom chip designs to perform specific functions.

Paragraph 57 on page 11 is amended as follows:

FIG. 17 illustrates a feasibility assessment result using the methodology shown in FIG. [2]16.

Paragraph 74 on page 11 is amended as follows:

FIG. 34 [is a flowchart illustrating the collaring process]illustrates a combination of the features illustrated in FIGS. 32 and 33.

Paragraph 80 on page 12 is amended as follows:

FIG. 40 shows a [computer]system [for performing the steps in the collaring process of]design using a collaring process such as that illustrated in FIG. 34.

The header on page 85, line 1 is amended as follows:

[Using]DFT Rules

Paragraph 114 on pages 14-15 is amended as follows:

To overcome the shortcomings of the available art, a novel methodology and implementation for block-based design ("BBD") is disclosed herein. In one or more preferred embodiments as described herein, both programmable and non-programmable circuit components can be utilized in a circuit block. FIG. 1, as will be described in more detail, illustrates a top-level overview of a block-based design process. The other figures provide further details relating to embodiments or implementations of various block-based design processes in accordance with the general framework

shown in FIG. 1. FIGS. 74-8[ ]7, in particular, are described with particular focus on the use of programmable circuitry in the block-based design process.

In the Claims

Claims 2-9, 11, 13-20, and 22 are amended as follows:

2. (Amended) A method for [designing]creating a derivative circuit [block]design, comprising:

(a) selecting an original circuit design, wherein the original circuit design comprises one or more programmable fabrics;

(b) performing front-end acceptance testing on the original circuit design;

(c) planning a chip layout;

(d) programming at least one of the one or more programmable fabrics to create a derivative circuit design; and

(e) performing verification [of]analysis on the derivative circuit [block]design.

3. (Amended) The method of claim 2, wherein the [step of planning the chip layout does not result in altering the]chip layout does not exceed bounds dictated by the front-end acceptance testing.

4. (Amended) The method of claim 2, further comprising the step of performing clocking and timing analysis prior to the step of performing verification [of]analysis on the derivative circuit [block]design.

5. (Amended) The method of claim 2, further comprising the step of performing power analysis prior to the step of performing verification [of]analysis on the derivative circuit [block]design.

6. (Amended) The method of claim 2, wherein only a set of new functionality added to the original circuit design and any functionality interfacing with the set of new functionality is tested or verified.

7. (Amended) The method of claim 2, wherein step [A](a) through step [E](e) are repeated to [design]create a second derivative circuit design, such that the original circuit design [of the second derivative circuit design is]comprises a derivative circuit design.

8. (Amended) The method of claim 2, wherein the step of planning the chip layout comprises[:] analyzing timing requirements to ensure the derivative circuit [block]design meets all applicable timing requirements.

9. (Amended) The method of claim 2, further comprising the step of assembling [the]a chip based on the chip layout prior to the step of performing verification [of]analysis on the derivative circuit [block]design.

11. (Amended) The method of claim 10, wherein each of the one or more programmable fabrics [each]has a port access and hierarchical routing.

13. (Amended) A computer readable medium carrying one or more sequences of one or more instructions for [designing]creating a derivative circuit [block]design, wherein the execution of the one or more sequences of the one or more instructions causes the one or more processors to perform the steps of:

(a) selecting an original circuit design, wherein the original circuit design comprises one or more programmable fabrics;

(b) performing front-end acceptance testing on the original circuit design;

(c) planning a chip layout;

(d) programming at least one of the one or more programmable fabrics to create a derivative circuit design; and

(e) performing verification [of]analysis on the derivative circuit [block]design.

14. (Amended) The computer readable medium of claim 13, wherein the [step of planning the chip layout does not result in altering the]chip layout does not exceed bounds dictated by the front-end acceptance testing.

15. (Amended) The computer readable medium of claim 13, further comprising the step of performing clocking and timing analysis prior to the step of performing verification [of]analysis on the derivative circuit [block]design.

16. (Amended) The computer readable medium of claim 13, further comprising the step of performing power analysis prior to the step of performing verification [of]analysis on the derivative circuit [block]design.

17. (Amended) The computer readable medium of claim 13, wherein only a set of new functionality added to the original circuit design and any functionality interfacing with the set of new functionality is tested or verified.

18. (Amended) The computer readable medium of claim 13, wherein step [A](a) through step [E](e) are repeated to [design]create a second derivative circuit design, such that the original circuit design [of the second derivative circuit design is]comprises a derivative circuit design.

19. (Amended) The computer readable medium of claim 13, wherein the step of planning the chip layout comprises[:] analyzing timing requirements to ensure the derivative circuit [block]design meets all applicable timing requirements.

20. (Amended) The computer readable medium of claim 13, further comprising the step of assembling [the]a chip based on the chip layout prior to the step of performing verification [of]analysis on the derivative circuit [block]design.

22. (Amended) The computer readable medium of claim 21, wherein each of the one or more programmable fabrics [each]has a port access and hierarchical routing.